Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VOUT SENSE**
2. **ADJ**
3. **VOUT**
4. **VIN**
5. **VOUT**

**.103”**

**MASK**

**REF**

**5 3**

**4**

**1**

**2**

**1086B**

**.085”**

**NOTE: CONNECT VOUT SENSE TO BACKSIDE**

**SUBSTRATE FOR CORRECT OPERATION**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .007 x .007” min.**

**Backside Potential: VOUT**

**Mask Ref: 1086B**

**APPROVED BY: DK DIE SIZE .085” X .103” DATE: 1/12/22**

**MFG: LINEAR TECH THICKNESS .012” P/N: LT1086**

**DG 10.1.2**

#### Rev B, 7/1